IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:Sakae KOYATA et al.	Group Art Unit : 1792
Appl. No.	: 10/562,236	Examiner : Kin Chan Chen
Filed	: February 7, 2007	Confirmation No. : 3799
For	: MANUFACTURING METHOD OF SILICON WAFER	

CORRECTED CLAIM OF PRIORITY

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop **Issue Fee**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

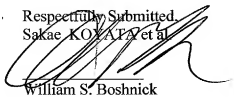
Further to the Claim of Priority filed with International Application No. PCT/JP04/16001 of which the present application is the U.S. national stage and incorrectly included in the executed Declaration filed February 7, 2007, Applicants hereby claim the right of priority granted pursuant to 35 U.S.C. 119 and 365 based upon Japanese Application No. 2003-401657, filed December 1, 2003, which priority is correctly indicated on the Official Filing Receipt. As required by 37 C.F.R. 1.55, a certified copy of the Japanese application has been received in this national stage application from the International Bureau.

Moreover, Applicants are submitting on even date herewith a Supplemental Declaration including the corrected priority information.

Authorization is hereby provided to charge any required fee for entry and/or consideration of this paper to Deposit Account No. 19-0089.

Should there be any questions, the undersigned can be reached at the below identified telephone number.

Respectfully Submitted,
Sakae KOYAMA et al.



William S. Boshnick
Reg. No. 44,550

September 22, 2009
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191

Arnold Turk
Reg. No. 33094